REMARKS

Claims 1-28 remain pending. Claims 1, 2, 5, 16, 18, 19, 22, 26-28 have been amended.

The Examiner has objected to drawings 5-8A and 9 under 37 CFR 1.84 or 1.152. Applicant hereby elects under 37 CFR 1.85 to delay filing of the new drawings with the changes incorporated therein until receipt of a Notice of Allowability (PTOL-37).

The Examiner has objected to the Abstract of the Disclosure as being written in more than a paragraph. Accordingly, it is requested that the Examiner amend the Abstract of the Disclosure into a single paragraph by removing the spaces and carriage return between lines 11 and 13 on page 24 of the specification. In addition, please also amend the word "coincidental" on line 19 of the same page to "coincident" for the reasons provided in the discussion below.

With regard to the position that the several "voltage pulse" recitations are unclear, which eventually led to the objection of claims 1-25 by the Examiner, claims 1, 5, 22, 26, and 27 have been amended to distinguish the different voltage pulses consistent with the other pending claims. For example, some of the "voltage pulse" recitations associated with the source of a semiconductor device are: "voltage pulse at the source of the semiconductor device"; "third voltage pulse"; "fourth voltage pulse"; and "constant positive voltage pulse". As another example, some of the "voltage pulse" recitations associated with the gate of the semiconductor device are: "multiple step voltage pulse"; "first voltage pulse"; "second voltage pulse"; "first negative voltage pulse"; and "second negative voltage pulse". Furthermore, as the Examiner presumed, the "said multiple voltage pulse" in claim 1 should be "said multiple step voltage pulse". Appropriate amendment has been made in order to establish a clear antecedent basis.

The Examiner was also unclear about "the first and second time intervals are substantially coincidental" language previously cited in claim 2. Accordingly, the "coincidental" language in claim 2 has been amended to "coincident" to further reflect a coexistence in time and avoid any interpretation of it being accidental. That is, the first and second time intervals of their respective "first and second voltage pulses" of the multiple step voltage pulse that is applied to the gate of a semiconductor device are substantially coincident (e.g., occur concurrently) in time with the application of the "voltage pulse at the source of the semiconductor device". Therefore, the first and second time intervals which are associated with the "first and second voltage pulses" applied to the gate of a semiconductor device are separate time intervals from the time interval associated with the "voltage pulse at the source of the semiconductor device". However, the application of both the "first and second voltage pulses" occupies substantially the same space in time with the application of the "voltage pulse at the source of the semiconductor device".

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The Examiner rejected claims 1-15 under 35 U.S.C. §102(a) as being anticipated by U.S. Patent Number 6,005,809 (Sung et al) or U.S. Patent Number 5,991,205 (Hara). Since these cited patents were not issued (Sung et al – December 21, 1999; Hara – November 23, 1999) until after the filing date of the Applicant's application for patent (August 16, 1999), neither Sung et al. nor Hara constitute prior art under 35 U.S.C. §102(a). Nevertheless, they may be prior art under 35 U.S.C. §102(e) and will be addressed below.

It is respectfully submitted that the cited art fails to describe or suggest a method for improving the source leakage of flash EPROM cells during source erase in the manner claimed. Independent claim 1 is directed towards "a method for erasing a semiconductor device". Claim 1 also requires "applying a voltage pulse at the source of the semiconductor device". Claim 1 also requires "applying a multiple step voltage pulse of the opposite polarity, said multiple step voltage pulse having at least a first voltage pulse and a second voltage pulse, at the gate of the semiconductor device" wherein "said second voltage pulse is greater in magnitude than said first voltage pulse". That is, the applied gate voltage pulse magnitude is varied during source erase while the applied source voltage pulse magnitude is substantially held constant. As a result, the present invention offers the advantage of faster source erase with a high magnitude voltage pulse and low source diode leakage. Furthermore, the method of the current invention is most useful in modern semiconductor devices of decreasing channel length where the capacity of source charge pumps is particularly limited.

Although Sung et al. teaches an erase method in general, Sung et al. fails to teach or suggest the above described erase method of applying varying magnitude voltage pulses in the manner claimed. Sung et al. merely teaches applying a constant magnitude voltage to not only the gate and the source, but also the substrate of a semiconductor device. As a result, erasure is achieved by forcing electrons from the floating gate to the control gate whereas in the pending patent application, erasure is achieved by forcing electrons from the floating gate to the source. Thus, it is respectfully submitted that Sung et al. fails to teach or suggest an erase method of applying varying magnitude voltage pulses to the gate of a semiconductor device while applying a substantially constant magnitude voltage pulse to the source of a semiconductor device. For this reason, it is submitted that independent claim 1 is patentable over Sung et al.

Hara teaches an erase method in general as well. However, like Sung et al., Hara fails to teach or suggest the above described erase method of applying varying magnitude voltage pulses in the manner claimed. Hara merely teaches applying a constant magnitude voltage to not only the gate and the source, but also the N and P wells of a semiconductor device. Thus, it is respectfully submitted that Hara also fails to teach or suggest an erase method of applying varying magnitude voltage pulses to the gate of a semiconductor device while applying a

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substantially constant magnitude voltage pulse to the source of a semiconductor device. For this reason, it is submitted that independent claim 1 is patentable over Hara.

The Examiner's rejections of the dependent claims are respectfully traversed. However, to expedite prosecution, all of these claims will not be argued separately. Claims 2-15 each depend either directly or indirectly from independent claim 1 and, therefore, are respectfully submitted to be patentable over cited art for at least the reasons set forth above with respect to claim 1. Further, the dependent claims require additional elements that when considered in context of the claimed inventions further patentably distinguish the invention from the cited art.

For example, claim 2 requires that the multiple step voltage pulse comprises "applying the first voltage pulse for a first time interval". Claim 2 also requires "applying the second voltage pulse for a second time interval" wherein "the first and second time intervals are substantially coincident with applying the voltage pulse at the source of the semiconductor device". In other words, two separate voltage pulses ("the first voltage pulse" and "the second voltage pulse") are applied to the gate of the semiconductor device at two separate time intervals that are substantially coincident with the time interval of applying the voltage pulse at the source of the semiconductor device. Claims 13 and 15 further require that "the first time interval is about 300 μsec" and that "the second time interval is about 200 μsec" respectively. The Examiner has pointed to the cited art as teaching the use of pulses for memory erase systems. However, the cited art fails to teach the application of a multiple step voltage pulse with separate time intervals for each voltage pulse that is comprised within the multiple step voltage pulse. Instead, the cited art merely applies a constant voltage pulse throughout a single time interval. Accordingly, the cited art fails to teach or suggest a method for improving the source leakage of flash EPROM cells during source erase in the manner claimed.

Applicant believes that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below. If any fees are due in connection with the filing of this paper, the Commissioner is hereby authorized to charge such fees to deposit account number 50-0388 (Order No. ALSCP003).

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP

James E. Austin
Reg. 39,489

P.O. Box 130
Mountain View, California 94042
(510) 843-6200

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